AMENDMENTS TO THE SPECIFICATION

Please add the following new paragraph after the paragraph beginning at line 18 of page 6:

FIG. 5 is a schematic diagram showing an LCD circuit according to another embodiment of the invention.

Please replace the paragraph between page 6, line 21 and page 7, line 11 with the following rewritten paragraph:

Referring to FIGS. 1, 2, and 4, ~~FIG. 1 and 2 are a schematic and a sectional view showing~~ the structure of a TFT-LCD is shown according to one embodiment of the invention, wherein some sub-pixels of a display region indicated by dashed lines in FIG. 4 are exemplified by those shown in FIG. 1. As shown in FIG. 1, the TFT-LCD includes an array substrate 12 on which pixel electrodes 10 are formed in a matrix and a facing substrate 14 arranged so as to face the array substrate surface at a predetermined interval. A TFT 16 serving as a switching element is formed near the pixel electrodes 10 on the array substrate 12 of the TFT-LCD respectively and source electrodes 18 of these TFTs are connected to the pixel electrodes 10. A gate electrode 20 and a drain electrode 22 of a TFT are connected to the scan signal line 24 and data signal line 26 for receiving scan signals SS and data signals DS from the scan driver SD and data driver DD constituting a row and a column of a matrix respectively. The scan signal lines 24

and the data signal lines 26 are formed at predetermined intervals and they are all perpendicular to each other. Moreover, each pixel electrode 10 has a necessary capacitance between the pixel electrode 10 and the storage capacitance line 28. This capacitance serves as a storage capacitance 29.

Please replace the paragraph between page 7, line 12 and page 8, line 26 with the following rewritten paragraph:

As shown in FIG. 2, an existing TFT-LCD has a structure in which an undercoat layer 42, a gate electrode 20 (scan signal line 24), a pixel electrode 10, a gate insulating film 44, a semiconductor layer (channel layer) 46, a channel protective film 48, an ohmic contact layer 50, a passivation film 52, and an alignment film 54 are deposited on an array substrate 12. Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD corresponding to an area in which pixel electrodes 10 on the array substrate 12 are arranged in a matrix. ~~I16ut~~ Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is

supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electrical resistance, the electrical resistance from a potential supply terminal to the central portion of a display screen increases as a display unit increases in size. Moreover, in the case of a color-display TFT-LCD, a color filter 32 consisting of three primary colors of red (R), green (G), and blue (B) is formed in a matrix between the facing substrate 14 and the common electrode 30 corresponding to the pixel electrode 10 of the array substrate 12. Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing film 38 is frequently set at the outer laterals of the array substrate 12 and the facing substrate 14. Furthermore, a direct-view transmission-type TFT-LCD has a backlight 68 and an image is output by controlling the transmittance of an incident light 69 emitted from the backlight 68.

Please replace the paragraph between page 8, line 27 and page 9, line 12 with the following rewritten paragraph:

FIG. 4 shows the LCD circuit on the array substrate 12. In addition to scan signal lines, data signal lines, storage capacitance lines (or called common voltage lines), and switching elements to form sub-pixels of the display device, an active matrix display device according to the invention, such as the TFT-LCD shown in this embodiment, includes test switches which are coupled to the scan signal lines and whose control terminals are coupled to the common voltage lines. When indicating enabling test switches, e.g. a high logic voltage level, the reference voltage can be applied to the control terminals to enable the test switches for transferring test signals applied to the test switches through the scan signal lines to the sub-pixels so as to perform a test of the display device. Conversely, when indicating disabling test switches, e.g. a low logic voltage level, the reference voltage can be applied to the control terminals to disable the test switches while the reference voltage serves as a common voltage to be supplied on the common voltage lines, that is, the storage capacitance lines, so as to enable storage capacitance to be formed within the sub-pixels. In FIG. 4, ~~Test~~ test transistors NL1~NL4 equal to the number of rows of pixels are formed next to the pixel array PA on the array substrate 12 and

used as test switches for the light-on test. The test transistors NL1~NL4 have drains/sources coupled to the scan signal lines 24, sources/drains coupled to receive a LCDQ2 signal and gates coupled to receive a LCDQ1 signal. The test transistors NL1~NL4 are turned on by the signal LCDQ1 so that the signals LCDQ2 are transmitted on the scan signal lines 24 to illuminate the pixels during the light-on test. The transistors NL1~NL4 are turned off by the signal LCDQ1 so that the signals LCDQ2 isolated from the scan signal lines 24 and the signal LCDQ1 is used as the common voltage Vcom supplied to the storage capacitors 29 in the pixels through the storage capacitance lines 28 beyond the light-on test.

Please replace the paragraph between page 9, line 18 and page 10, line 2 with the following rewritten paragraph:

Alternatively, the test transistors NL1~NL4 may have drains/sources coupled to the data signal lines 26 instead of the scan signal lines 24, or, in addition to the test transistors NL1~NL4, there may be test transistors having drains/sources coupled to the data signal lines 26. As exemplified in FIG. 5, in addition to the first group of test transistors NL1 to NL4, a second group of test transistors NC1 to NC4 are coupled to the data signal lines, and their control terminals, that is, gates of the test transistors NC1 to NC4, are coupled to the common voltage lines. In FIG. 5, a gate of one of the test transistor NL1 of the

first group of test transistors and a corresponding common voltage line 28 are connected to a first input terminal, denoted by T1, while a gate of one of the test transistor NC1 of the second group of test transistors and a corresponding common voltage line 28 are connected to a second input terminal, denoted by T2. In FIG. 5, all of these first input terminals T1 corresponding to the test transistors NL1 to NL4 are connected to a conducting line LL. All of these second input terminals corresponding to the test transistors NC1 to NC4 are connected to the conducting line LL, for example. One of the second group of test transistor, for example NC1, when enabled through its second input terminal T2, causes a second test signal, denoted by LCDQ3, to feed to a corresponding data signal line DS. According to FIG. 4 or 5, the display region indicated by dashed lines in FIG. 4 or 5 includes a plurality of pixels or sub-pixels and can be regarded as being composed of a plurality of blocks. Each of the blocks, or called a sub-pixel section, corresponds to some test transistors, such as NL1 to NL4, and corresponds to a set of input terminals, such as the input terminals T1 corresponding to NL1 to NL4. Further, this circuit configuration is suitable for a normally white pixel array. The common voltage is provided by the LCDQ signal which is different from the voltage on the common electrode of the facing substrate. By shorting the switching transistor to the common voltage line to bypass the storage capacitor, the voltage difference between the common electrodes of the array and facing

substrate turns a defect pixel to a dark pixel. Thus, there is no white pixel even if there are defects in a normally white pixel array.